# SEED LAYER FORMATION

## Field of the Invention

**[0001]** This invention relates to integrated circuit metallization processes, and particularly to the formation of a seed layer that is utilized for deposition of bulk copper.

## Background of the Invention

**[0002]** Metallization is the process that forms the interconnections of the components on an integrated circuit (IC). This can be accomplished by the deposition of a thin layer of a metal over the entire surface of the IC and then etched in a desired pattern. Until recently, the metal has commonly been aluminum, because dry etch processes are available for aluminum. Since the development of chemical mechanical polishing (CMP) techniques for the more conductive copper, damascene processing is rapidly gaining in acceptance. In damascene processes, a thick dielectric layer is patterned with trenches and/or vias, metal is blanket deposited over the substrate and into the openings, and excess metal is polished away from the top surfaces of the dielectric. This leaves metal inlaid within the trenches and/or vias. In order for the metal, typically copper, to be properly laid there must be an appropriate surface for the copper to adhere to. Copper can be deposited by chemical vapor deposition (CVD) or plating, but in either case a suitable seed layer is typically formed lining the openings prior to bulk copper deposition.

**[0003]** Because of its high electrical conductivity and good electromigration properties, copper, rather than aluminum, is preferred in modern integrated circuits. Ohmic losses of the conductors are decreased because copper has a much higher conductivity than aluminum. The lower resistance and the associated ohmic losses are beneficial in photovoltaic applications in addition to analog and digital microcircuits and microprocessors. Copper-metallized microcircuits can accommodate higher currents because of copper's higher resistance to electromigration. Additionally, copper's properties allow the use of narrower and thinner conductors and interconnections. Furthermore, since tighter packing density can be obtained with copper, fewer metallization levels are typically needed for equivalent circuit designs using copper interconnects and, thus, the manufacturing costs can be lower than with aluminum.

[0004] However, copper's benefits are also balanced by some problems. A major problem associated with using copper is that it diffuses readily in common insulating materials. Therefore, great care has to be taken in order to prevent direct contact between copper and typical silicon oxide-based insulating layers. If this were to occur in an IC, it would cause short circuits. In order to prevent such diffusion, a barrier layer is generally introduced between the insulator and copper. This barrier layer, called a diffusion barrier, is deposited over the insulator surface before copper deposition, or over copper lines prior to insulator deposition. Some examples of relatively conductive barrier layers include tungsten, molybdenum, and titanium compounds, such as nitrides and carbides.

[0005] The atomic layer deposition (ALD) method of depositing thin films, such as diffusion barriers, has several attractive features including excellent step coverage, even on large areas, and a dense and pinhole-free structure. Therefore, it is also of great interest to apply ALD to the deposition of metallization layers of advanced integrated circuits (ICs), where the continuously increasing packing density and trench/via aspect ratios set higher demands upon the metallization layers. Applications where high quality metallization is particularly needed are dual damascene structures, gates in transistors and capacitor electrodes in ICs. However, due to the fact that ALD is based on sequential self-saturating surface reactions of source chemical compounds, depositing high quality elemental metal thin films by ALD is very difficult.

[0006] Metal oxide thin films produced by ALD, on the other hand, can be very uniform, have excellent adhesion and thus can be firmly bonded to the substrate surface. ALD metal oxide thin films can be used to make conductive thin films through oxidation state reduction after deposition of a metal oxide thin film. For example, Soininen et al., used an ALD deposited metal oxide thin film in order to produce a conductive thin film. (U.S. Pat. No. 6,482,740). After the ALD metal oxide thin film was produced, it was reduced by using organic compounds with at least one of the following functional groups: -OH, CHO, and –COOH, thus producing a metal thin film layer. Films of this process include both metal and conductive metal oxide films from various elements, including cobalt, copper, gold, nickel, osmium, platinum, rhenium, ruthenium, and silver.

[0007] One of the most advanced IC structures is the dual damascene structure over a semiconductor substrate with transistors (including source, gate and drain). Several

electrically conducting layers are needed in the structure. The first metallization level is conventionally fabricated with tungsten plugs and aluminum interconnects to prevent the contamination of the gate with copper. The remainder of the metallization levels are preferably made of copper.

**[0008]** Metallization of the trenches and vias can be attained by copper electroplating. Alternatives are electroless plating, physical vapor deposition (PVD), and CVD. A seed layer, usually deposited by CVD or PVD, is typically needed for electroplating processes. In the electroplating process the substrate having an electrically conductive seed layer is immersed in a metal compound solution. The electrically conductive surface of the substrate and an opposing electrode are connected to an external DC power supply. A current passes through the substrate surface into the solution and metal is deposited on the substrate. The seed layer has high conductivity and it acts as a conduction and nucleation layer for the electroplating process. A first seed layer can also act as a nucleation layer for the CVD process that forms a subsequent electroplating seed layer. The electroplating seed layer carries current from the edge of the wafer to the center of the wafer and from the top surface of the wafer into the bottom of vias and trenches, so it must be conductive. A uniform and continuous seed layer is desirable to produce uniform electroplated copper. The quantity of the deposited metal is directly proportional to the local current density on the substrate.

**[0009]** It has been complicated to form a sufficiently uniform copper seed layer on a diffusion barrier in high aspect ratio trenches and vias. For example, in the process of U.S. Patent No. 6,482,740, the process window of ALD-grown copper oxide is rather narrow. In that process, copper oxide is reduced into elemental copper metal in a subsequent process step. Direct growth of elemental copper using ALD chemistry is also rather complicated, and it can contaminate the ALD reactor chamber. Other materials have been tried in place of a copper seed layer. Copper will grow evenly on these non-copper seed layers, but there are drawbacks to these chemicals as well. For example, ruthenium makes an excellent seed layer. Additionally, it will bond well to the surface of a barrier layer such as tungsten nitride carbide ($WN_xC_y$, wherein x and y denote a range of chemical compositions including non-stoichiometric compounds). However, the growth of a ruthenium seed layer can itself be a very time consuming process, as the incubation or nucleation period of the ruthenium is quite long.

[0010] It is accordingly an objective of the present invention to avoid these and other disadvantages and to facilitate the process of metallizing dual damascene structures. There is a need for better and more efficient seed layers for the deposition of metals for the purpose of metallizing ICs.

## Brief Summary of the Invention

[0011] According to one aspect of the invention, a method for metallizing an integrated circuit is provided. The method comprises depositing a diffusion barrier on a substrate. A top layer of the diffusion barrier is oxidized to form a metal oxide layer. The oxidation state of the metal oxide layer is preferably reduced in order to form a seed layer. A conductor is then deposited directly over the seed layer.

[0012] In a preferred embodiment, the diffusion barrier layer is tungsten nitride carbide or molybdenum nitride carbide.

[0013] According to another aspect, a method for metallizing an integrated circuit comprises forming a diffusion barrier layer on a substrate and performing a preparation process on the substrate to form a nucleation layer. Ruthenium is then deposited of the nucleation layer to form a second seed layer. Copper is then deposited over the second seed layer.

[0014] Preferably, the preparation process is repeated before depositing a conductive layer to form a seed layer. In a preferred embodiment, the preparation process comprises exposing the substrate to pulses of oxygen and hydrogen and the conductor is ruthenium.

[0015] In another aspect, another method of metallizing an integrated circuit comprises forming a tungsten nitride carbide diffusion barrier on a substrate. A tungsten oxide layer is then formed over the diffusion barrier. The tungsten oxide layer is reduced to form a first seed layer before depositing a copper layer over the first seed layer.

[0016] In another aspect of the invention, a metallization structure comprises a diffusion barrier including a metal and deposited by atomic layer deposition, a nucleation layer formed from the metal in the diffusion barrier layer, and a ruthenium seed layer deposited by ALD over the nucleation layer.

[0017] In another aspect, a metallization structure in an integrated circuit comprises a diffusion barrier, a first seed layer directly over the diffusion barrier formed from the same metal as the diffusion barrier, and a copper layer over the first seed layer.

[0018] In a preferred embodiment of the above aspect of the invention, there is a second seed layer between the first seed layer and the copper layer. Preferably this second seed layer is ruthenium.

## Brief Description of the Drawings

[0019] These and other aspects of the invention will be better understood from the Detailed Description of the Preferred Embodiments and from the appended drawings, which are meant to illustrate and not to limit the invention, and wherein:

[0020] Figure 1a is a schematic, cross-sectional side view of a substrate with a diffusion barrier on top in accordance with a starting step for a preferred embodiment of the present invention.

[0021] Figure 1b is a schematic, cross-sectional side view of the substrate of Figure 1a after a layer of metal oxide has been formed over the diffusion barrier.

[0022] Figure 1c is a schematic, cross-sectional side view of the substrate of Figure 1b after the metal oxide has been reduced to a conductive metal oxide or an elemental metal.

[0023] Figure 1d is a schematic, cross-sectional side view of the substrate of Figure 1c after copper has been deposited.

[0024] Figure 2a is a schematic, cross-sectional side view of a substrate with a diffusion barrier on top in accordance with a starting step for another preferred embodiment of the present invention.

[0025] Figure 2b is a schematic, cross-sectional side view of the substrate of Figure 2a after a nucleation layer has been formed over the barrier layer, similar to the seed layer of Figure 1c.

[0026] Figure 2c is a schematic, cross-sectional side view of the substrate of Figure 2b after a ruthenium seed layer has been deposited over the nucleation layer.

[0027] Figure 2d is a schematic, cross-sectional side view of the substrate of Figure 2c after copper has been deposited.

[0028] Figure 3a is a schematic, cross-sectional side view of a dual damascene structure with a diffusion barrier, first seed layer, second seed layer, and copper.

[0029] Figure 3b is a schematic, cross-sectional side view of the dual damascene structure of Figure 3a after a chemical mechanical planarization process.

[0030] Figure 4 is a flow chart of a process for metallizing a circuit with a preferred embodiment of the invention.

[0031] Figure 5 is a flow chart of a process for metallizing a circuit with another preferred embodiment of the invention.

[0032] Figure 6 is a flow chart of a process for metallizing a circuit with another preferred embodiment of the invention.

## Detailed Description of the Preferred Embodiments

[0033] In the illustrated embodiments, the metallization process is simplified because the direct or indirect deposition of a copper-containing seed layer can be eliminated from the process steps. Additionally, copper contamination of chemical vapor deposition (CVD) and atomic layer deposition (ALD) reactors is avoided.

[0034] According to an embodiment of the present invention as shown in FIG. 4, a diffusion barrier is deposited 10 on a substrate (e.g., semiconductor wafer). Preferably, a barrier layer such as tungsten nitride carbide or molybdenum nitride carbide can be deposited by ALD. A metal oxide is then formed 14 on the diffusion barrier layer. The metal oxide is preferably formed by oxidizing the surface of the diffusion barrier. The metal oxide is reduced 18 to a more conductive state in order to form a seed layer. This more conductive state can be a metal oxide with a lower oxidation state or an elemental metal. Copper is then deposited 25 over the seed layer. The elemental metal or conductive metal oxide serves as the seed layer when copper is deposited. Through this process, one of the critical steps in the metallization of an integrated circuit, the deposition of a copper-containing seed layer, can be eliminated.

[0035] According to another embodiment of the invention, a second seed layer (ruthenium in the illustrated embodiment) is deposited after a preparatory process, and the

preparatory process preferably comprises the repeated process of oxidization and reduction of the barrier layer to form a first seed layer. The first seed layer shortens the incubation time of the ruthenium ALD deposition. By decreasing the incubation time of a second seed layer, the total process time is reduced. In the illustrated embodiment, the preparatory process for forming the first seed layer comprises exposing a wafer that is coated with a barrier layer to alternating pulses of oxygen and hydrogen plasma. The second seed layer is preferably formed by depositing ruthenium by ALD after preparing a barrier-layer coated substrate. A process for depositing elemental ruthenium by ALD is disclosed in U.S. Patent Application No. 10/066,315, filed January 29, 2002, and published as US 2003/0165615 on September 4, 2003, disclosure of which is herein incorporated by reference. The ruthenium then serves as a seed layer for any copper that is to be deposited on the substrate.

**[0036]** The formation of seed layers and the subsequent metallization is particularly important in the context of a dual damascene structure. ALD can form high quality and very conformal thin films in damascenes, and the embodiments described can be applied to the damascene context.

The Formation of a Barrier Layer

**[0037]** As shown in FIG. 1a, a diffusion barrier 110 is deposited upon a substrate 112, preferably by atomic layer deposition (ALD). ALD is preferred for the conformity and quality of the thin films it produces. Preferably, the diffusion barrier is a metal nitride, such as tantalum nitride, e.g. TaN or $Ta_3N_5$, or a metal carbide, such as tungsten carbide, e.g $W_2C$ or WC, or their mixtures or nanolaminates, more preferably a metal nitride carbide. In two exemplary embodiments, the diffusion barrier is either tungsten nitride carbide ($WN_xC_y$) or molybdenum nitride carbide ($MoN_xC_y$). A process of forming thin films, such as the diffusion barrier, is disclosed in U.S. Patent Application Nos. 10/242,368, filed September 12, 2002, and published as 2003/0082296 on May 1, 2003, and 09/644,416, filed August 23, 2000, disclosures of which are herein incorporated by reference. The substrate could be a silicon wafer, or any other substrate.

**[0038]** The barrier layer 110 is preferably produced by an ALD process. ALD produces thin films with excellent step coverage. Step coverage is the ratio of thickness of the film at the bottom of the step to the thickness of the film at the upper surfaces of the step.

Good step coverage reduces electromigration and high-resistance pathways. ALD generally produces films with step coverage of greater than 95%. A typical ALD process comprises the following steps:

**[0039]** 1. placing a substrate into a reaction chamber;

**[0040]** 2. feeding into the reaction chamber and contacting the substrate with a pulse of at least one first source chemical, preferably in the vapor phase, under conditions such that no more than a molecular monolayer of the first source chemical adsorbs on the substrate;

**[0041]** 3. removing gases from the chamber;

**[0042]** 4. feeding into the reaction chamber and contacting the substrate with a pulse of at least one second source chemical, preferably in the vapor phase, comprising a compound capable of reacting with the adsorbed species of the first source chemical on the substrate;

**[0043]** 5. removing gases from the chamber; and

**[0044]** 6. repeating steps 2 through 5 until a desired thickness of the growing thin film is reached.

**[0045]** According to the ALD principles, the previous reactant (i.e. previously pulsed source chemical) and the gaseous by-products of the surface reaction are removed from the reaction chamber before the next pulse of a reactant is introduced into the reaction chamber. The reactants and the by-products can be removed from the reaction chamber by pumping down the chamber to a higher vacuum by a vacuum pump, by purging the chamber with an inert gas pulse, or by a combination of the two. Additional pulse and removal steps can be added to each cycle

**[0046]** A method of forming metal nitride carbide thin films, such as $WN_xC_y$ or $MoN_xC_y$, is disclosed in the '368 application incorporated above. For the deposition of $WN_xC_y$, the substrate temperature is preferably selected from a range of 275 – 350 °C, more preferably from a range of 300 – 325 °C. The W, N and C source chemicals for the deposition of $WN_xC_y$ are preferably tungsten hexafluoride ($WF_6$), ammonia ($NH_3$), and triethylboron (TEB), respectively. For $MoN_xC_y$, the sources for Mo, N, C are preferably molybdenum hexafluoride ($MoF_6$), ammonia ($NH_3$), and triethylboron (TEB), respectively.

The temperature values may also differ slightly. However, skilled artisans will appreciate that different source chemicals and temperature ranges can be used.

Oxidation of the surface of the barrier layer

**[0047]** In a preferred embodiment, the surface of the diffusion barrier 110 (FIG. 1a), preferably $WN_xC_y$ or $MoN_xC_y$, is next oxidized with an oxygen source chemical in order to create a metal oxide 122 (FIG. 1b), comprising tungsten oxide or molybdenum oxide for the exemplary embodiments. In some preferred embodiments this oxygen source could be air, diatomic oxygen ($O_2$), ozone ($O_3$), oxygen radicals ($O^*$), or hydrogen peroxide ($H_2O_2$). The oxidation can be performed as the result of being exposed to air in a clean room or other environment, but is preferably actively performed thermally and/or by exposure to radicals. The oxidation leaves a thinner diffusion barrier 114.

**[0048]** Another embodiment involves replacing the oxidation step 13 (FIG. 5) with the deposition 15 (FIG. 5) of the metal oxide 122 (FIG. 1b), preferably tungsten oxide or molybdenum oxide, by ALD on the diffusion barrier, which advantageously produces high quality, conformal films. Methods such as CVD can also be used to form a metal oxide film. However, the skilled artisan will recognize that other methods of depositing a metal oxide thin film may be used in the methods of the invention. The metal oxide 122 preferably includes a metal in common with the underlying barrier layer 114.

Reduction of the Oxide into a metallic seed layer

**[0049]** With reference to FIG. 1c, the metal oxide 122, preferably tungsten oxide or molybdenum oxide, is reduced into a conductive state to form a first seed layer 130. In preferred embodiments, the reduction is performed with hydrogen, hydrogen plasma, or carbon monoxide into a conductive metal oxide or elemental metal layer 130 that can be used as a seed layer. This can be seen in FIG. 1c. Surprisingly, reduction of tungsten oxide by thermal hydrogen can be accomplished at temperatures as low as 130°C. Of course, when the temperature is higher, the process time is shorter. For even shorter process time, in situ or remote hydrogen plasma can be used.

**[0050]** In another preferred embodiment, the metal oxide is electrochemically reduced to metal. A current is applied to the metal oxide in order to reduce it to the

elemental metal form. In this embodiment, the elemental metal, (e.g. tungsten or molybdenum) is then used as a seed layer for the deposition of copper for the vias and trenches.

**[0051]** Another embodiment is the reduction using a gaseous organic compound that contains one of the members of the following group: alcohol (-OH), aldehyde (-CHO), and carboxylic acid (-COOH). Reduction processes employing these organic reducing agents are described in U.S. Pat. No. 6,482,740, issued to Soininen, et al., and incorporated by reference herein. In a preferred embodiment using one of the above-named organic compounds, the metal oxide is reduced from a high oxidation state (such as $WO_3$) to a conductive low oxidation state (such as $WO_2$). The conductive low oxidation state metal is preferably used as a seed layer or further reduced using other reduction methods.

Second Seed Layer Process

**[0052]** As seen in FIGS. 2a-2d, another embodiment involves a second seed layer being deposited by an ALD process. Ruthenium, for example, can serve as a seed layer for subsequent CVD deposition of copper. However, the deposition of ruthenium via the ALD process is slow because of poor nucleation to the surface of layers such as $WN_xC_y$. To speed up the nucleation, the metal or metal oxide seed layer of the above process is preferably used as a nucleation layer for the ALD deposition of ruthenium. In order to increase the nucleation, additional cycles of oxidation and reduction are used in this preparation process. This process is outlined in the flow chart of FIG 6.

**[0053]** There are different forms of the preparation process for producing the first seed layer as a nucleation layer for depositing the second seed layer. Preferably the preparation process includes the combination of exposing the substrate to alternating pulses of oxygen and either in situ or remote hydrogen plasma or thermal hydrogen $H_2$, more preferably in situ plasma. Thus, the process of forming the metal or conductive metal oxide layer to be used as a nucleation layer above can be the first of these cycles.

**[0054]** In one embodiment, the substrate 212, which has been coated by a diffusion barrier 210 is repeatedly exposed to short pulses of oxygen and alternated with either in situ or remote hydrogen plasma. This process is then repeated *n* times. This forms a nucleation layer 232, and leaves a thinner original diffusion barrier layer 214. Here, *n* can

range from 1 to 100. In some embodiments the formed nucleation layer 232 is dense enough to act both as a nucleation layer and as a modified diffusion barrier layer resting on the original diffusion barrier layer 214. Generally, more cycles of this process leads to better nucleation and consequently, a lower sheet resistance and a thicker seed layer. In one embodiment, *n* is preferably between about 10 and 50, more preferably between about 20 and 40, and more preferably about 30. This allows for a balance between time in the preparation process and for time in the incubation time of the ruthenium seed layer. Each pulse can last less than a second or up to several minutes. The pulses of oxygen and hydrogen preferably last between about one second and one minute, more preferably between about 5 and 40 seconds, and most preferably between about 10 and 30 seconds. Regarding the deposition of ruthenium metal, reference is made to the U.S. Patent Application publication no. 2003/0165615, incorporated by reference herein above. Typical pulse times for the ruthenium and oxygen source chemicals are in the range of 0.5 – 1.5 s and 0.5 – 1.0 s, respectively. Purge periods between the reactant pulses are typically in the range of 0.5 – 2.0 s. The oxygen source flow rate is scaled according to the size of the substrates to be coated, and the $O_2$ flow rate can be selected e.g. from the range of about 5 – 100 std. $cm^3$/min (sccm).

**[0055]** In another embodiment, the preparation process includes exposing to a pulse of a ruthenium source chemical at the beginning of each cycle of the preparation process. The chamber is then purged, and the wafer is then exposed to oxygen. After another purge, the wafer is exposed to hydrogen plasma, either in situ or remote. This process is repeated *n* times, where *n* can range from 1 to 100. As seen in Fig 2c, ruthenium is further deposited (without the oxidation and reduction pulses) by ALD to form a seed layer 235 after the preparation process is complete.

Deposition of Copper

**[0056]** As shown in FIG. 1d and FIG. 2d, copper 140, 240 is deposited on a seed layer in order to complete the metallization of the circuit, preferably by electrochemical deposition. Alternatives are electroless plating, physical vapor deposition (PVD) and chemical vapor deposition (CVD). By using a conductive seed layer, such as a tungsten, molybdenum, or ruthenium, electroplating is possible and efficient. Copper can also be

deposited on the seed layer by CVD, PVD, and electroless plating methods. In any of these copper deposition processes, the trenches and vias are filled with bulk copper.

**[0057]** Preferably, the direct or indirect deposition of a copper-containing seed layer is avoided. By avoiding this step, the possibility of copper contamination of CVD and ALD reactors is significantly decreased. As described in U.S. Pat. No. 6,482,740, which was previously incorporated by reference, copper oxide deposition is a slow process; oxidation and reduction as described above can be more efficient and economical. Additionally, time is saved in the processing of a wafer by using the oxidation and reduction processes, as opposed to a separate deposition step, and the layer adhesion is seen to greatly improve.

**[0058]** As seen in FIG. 3a, the first seed layer 352 can be used as described above to be a nucleation layer for a ruthenium second seed layer 354. Copper filler 340 can then be deposited on the second seed layer 354. In some other embodiments copper filler 340 can also be deposited directly on the first seed layer 352, which is formed from the underlying diffusion barrier 350. Copper layers can be seen in FIGS 1d and 2d, as well as in the context of a dual damascene structure in FIGS 3a and 3b.

**[0059]** After the copper has been deposited, there will be several layers on the substrate. First, it will have a diffusion barrier layer 350, preferably $WN_xC_y$ or $MoN_xC_y$. It will then have a first seed layer 352 of a metal or a conductive metal oxide. If the ruthenium seed layer 354 and the associated preparation process are used, that first seed layer 352 will be used as a nucleation layer for the second seed layer 354 of ruthenium. The ruthenium seed layer 354 will have the features and benefits of an ALD-deposited thin film. Finally, a layer of copper filler 340 will be on top of these other layers.

Structure

**[0060]** In dual damascene structures, metallization is particularly important. The damascene structure can be seen in FIG. 3a with copper deposited into the damascene openings. A diffusion barrier layer 350 lines the walls of the trench, preferably $WN_xC_y$ or $MoN_xC_y$. A first seed layer 352 directly overlies the diffusion barrier 350. As discussed earlier, this first seed layer 352 is preferably made from the same metal as the diffusion barrier 350. The next layer is an optional second seed layer 354 made using the preferred embodiment discussed above. Finally, copper filler 340 fills the trench.

[0061] FIG. 3b is a drawing of the structure after a chemical mechanical polishing (CMP) or other planarization process. It is also possible to deposit a CMP stop layer on the top surface of the insulator 312 before etching the trenches and vias. A CMP stop layer (not pictured) can be any material with a smaller etch rate than the insulator 312, such as SiC. In another preferred embodiment, the diffusion barriers described herein are used as a CMP stop layer. The preferred materials for the diffusion barrier, $WN_xC_y$ and $MoN_xC_y$, are also used as etch stops in many applications. Using the diffusion barrier as the CMP stop layer saves a step over depositing a separate etch stop layer.

Example: Deposition of copper upon tungsten seed layer

[0062] A 20 nm thermal silicon oxide wafer was coated with 10 nm of $WN_xC_y$ and transported to another facility. During the process of transportation between the factories, 1.9 nm (19 Å) of the barrier layer $WN_xC_y$ was oxidized. The surface of this wafer was then reduced with in situ $H_2$ plasma using a power of 1500 W at 250°C for 30 seconds in an Eagle™ 10 reactor, available from ASM Japan K.K. of Tokyo, Japan. The wafer was again transported to another factory for the deposition of copper. About 50 nm of copper was deposited by using a metal organic chemical vapor deposition (MOCVD) Superfill deposition. After transportation back to the original facility, the wafer was tested by forming a 11 x 11 scratch grid with diamond-tipped pen and using the standard Scotch tape tests. This test revealed that the film did not delaminate, even after thermal cycling of 3 cycles of 1 minute at 400°C, with 5 minutes of cooling in between.

[0063] Thus, it could be seen that no copper seed layer is needed for CVD copper deposition if the $WN_xC_y$ surface is first oxidized by air or some other oxidant and then reduced into tungsten by a process such as using in situ hydrogen plasma. A similar method can be used in making seedless ECD copper deposition on a conductive tungsten surface. However, the seed layer should be thicker for ECD deposition, preferably by actively (thermally or by plasma) oxidizing the film prior to reduction.

[0064] Although the foregoing invention has been described in terms of certain preferred embodiments, other embodiments will be apparent to those of ordinary skill in the art. Additionally, other combinations, omissions, substitutions and modification will be apparent to the skilled artisan, in view of the disclosure herein. Accordingly, the present invention is not

intended to be limited by the recitation of the preferred embodiments, but is instead to be defined by reference to the appended claims.